EGC442
Class Notes
3/28/2023

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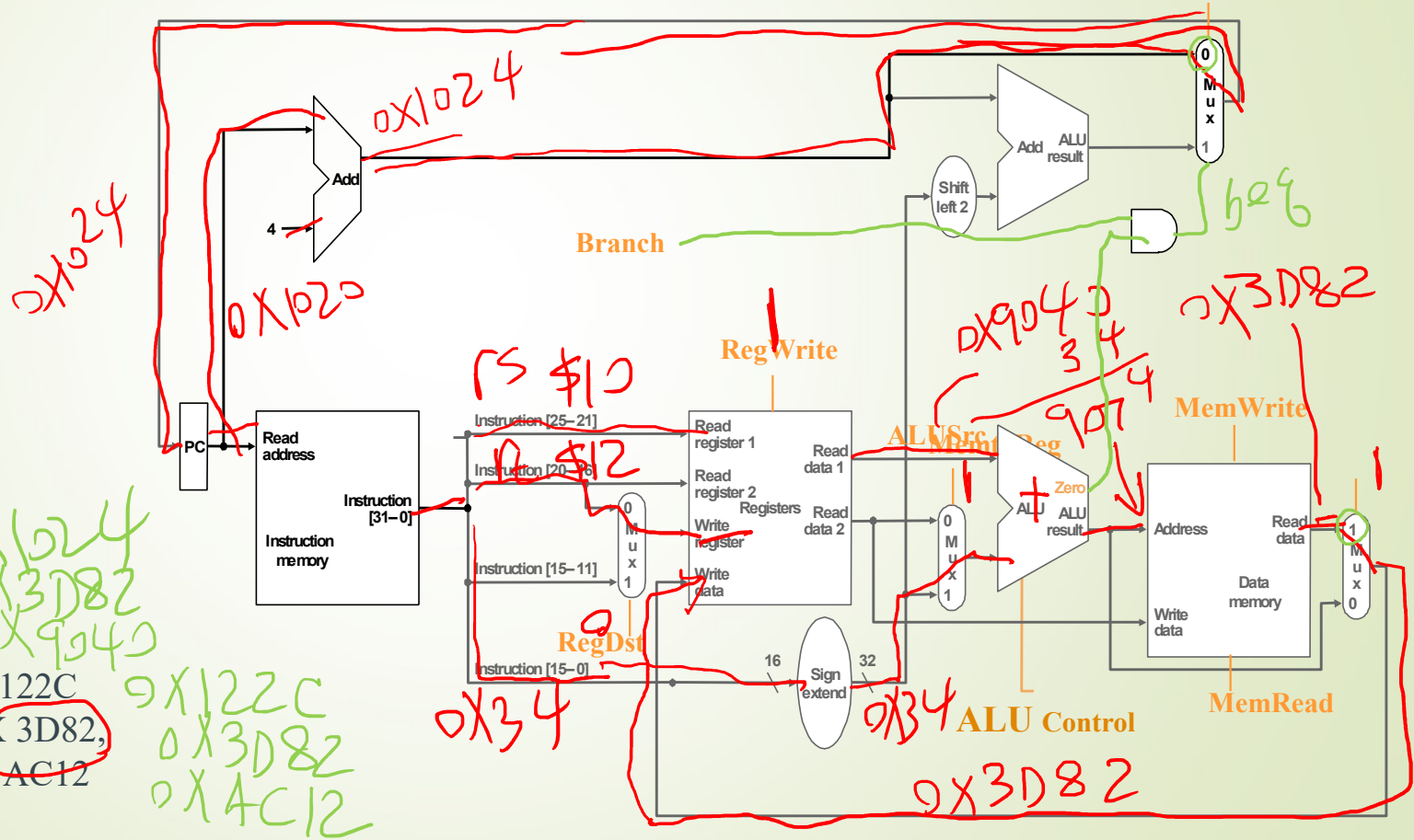
Problem 27) lw $12, 0x34 ($10)

Instruction	Opcode	RegDst	ALUSrc	Memto-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUOp0
lw	10 0011	0	1	1	1	1	0	0	0	0

ALU Control:
000 AND
001 OR
010 add
110 subtract
111 set-on-less-than



PC= 0X1020,
$12 = 0X9040
$10= 0X9040
Mem[0x9040]= 0X122C
Mem[0x9074] = 0X 3D82,
Mem[0x84B4]= 0x AC12

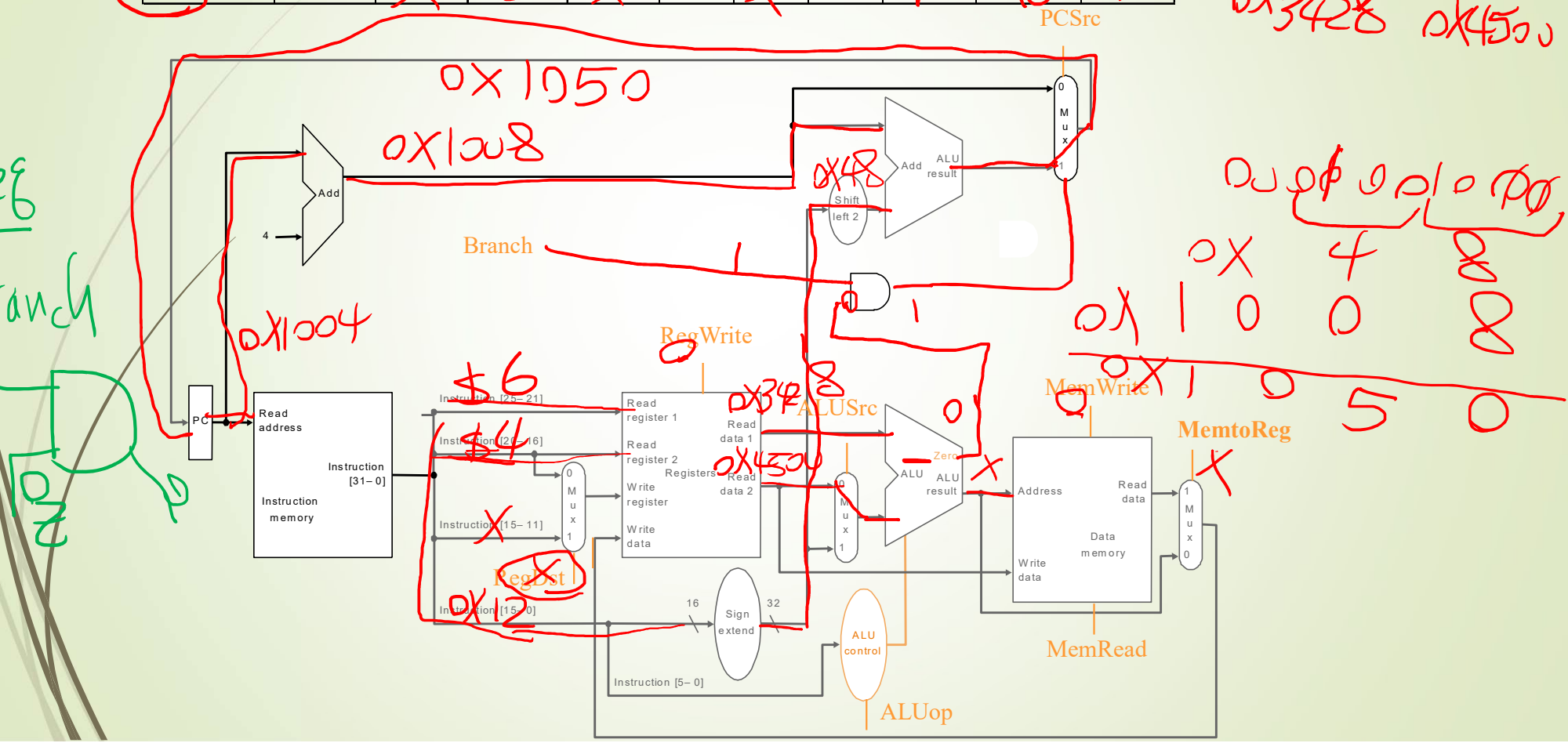
Instruction	Opcode	RegDst	ALUSrc	Memto-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUOp0
R-format	00 0000									
lw	10 0011	0	1	1	1	1	0	0	0	0
sw	10 1011									
bne	00 0100	X	0	X	0	X	0	1	0	1

bne $6, $4, 0x12

0x3428 0x4500

beq

branch



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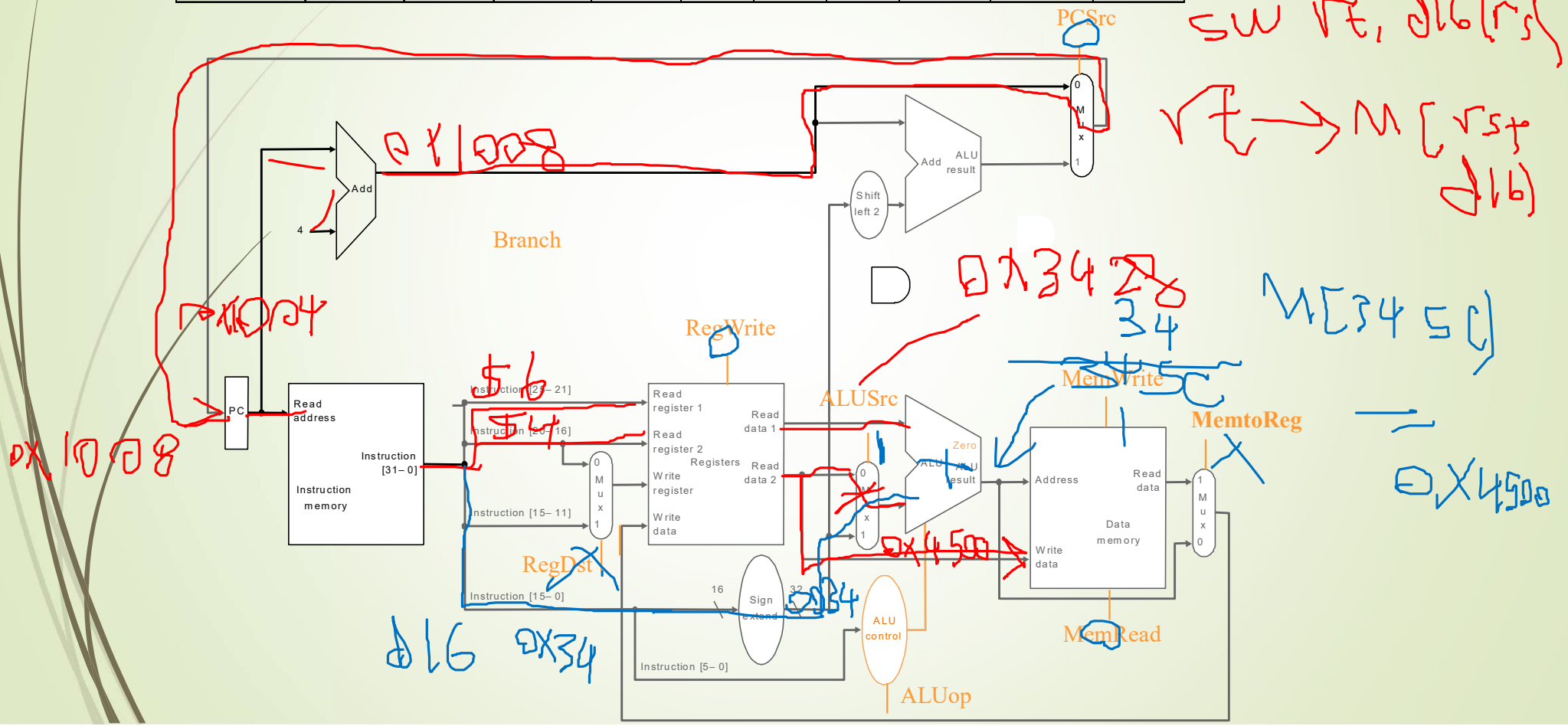
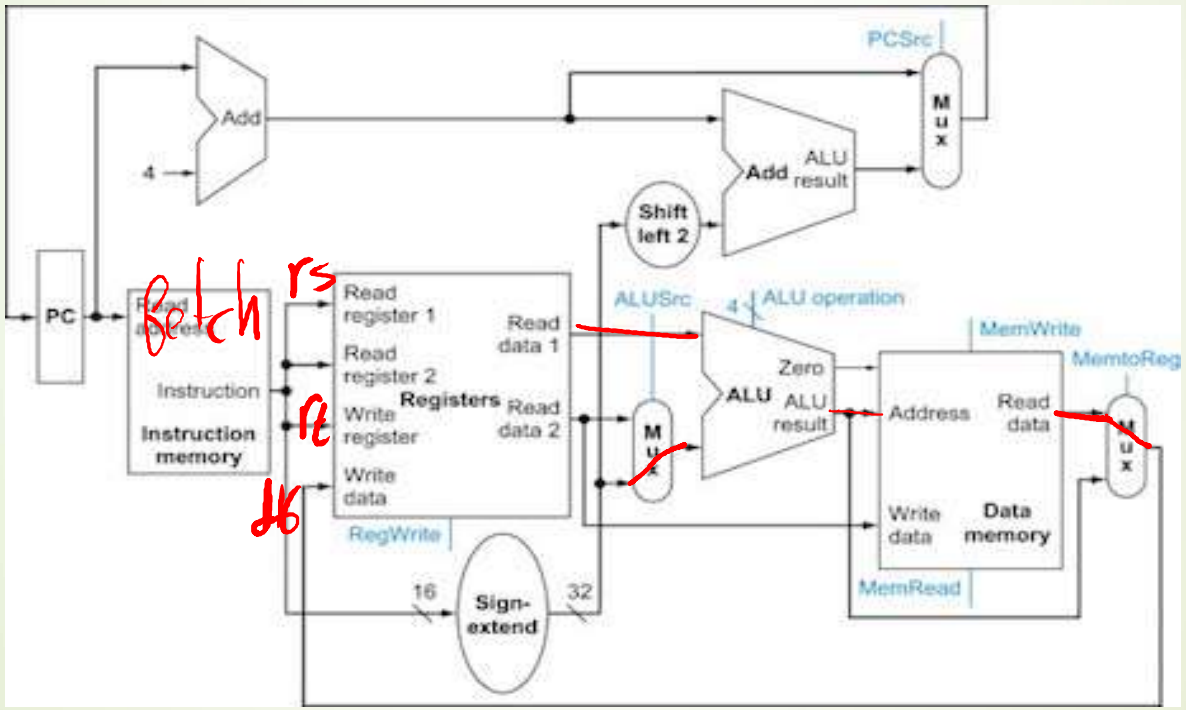
R-format	00 0000									
lw	10 0011									
sw	10 1011	X	1	X	0	0	1	0	1	0
bne	00 0100									



Which of the following is correct for a load instruction?

- MemtoReg should be set to cause the data from memory to be sent to the register file.
- MemtoReg should be set to cause the correct register destination to be sent to the register file.
- We do not care about the setting of MemtoReg for loads.



1) The single-cycle datapath conceptually described in this section *must* have separate instruction and data memories, because _____.

the formats of data and instructions are different in MIPS, and hence different memories are needed

having separate memories is less expensive

the processor operates in one cycle

1) If the instruction is SW, then ALUOp should be _____.

00

01

10

unknown

1) If the instruction is SW, then the ALU's four control inputs should be _____.

0000

0010

0110

1) For LW and SW instructions, the ALU function _____

is the same

differs

1) If the instruction is OR, then ALUOp should be _____.

0001

10

unknown

1) If the instruction is OR, then as well as examining the ALUOp bits, the ALU control will also examine _____.

Instruction[31:26] (the leftmost bits)

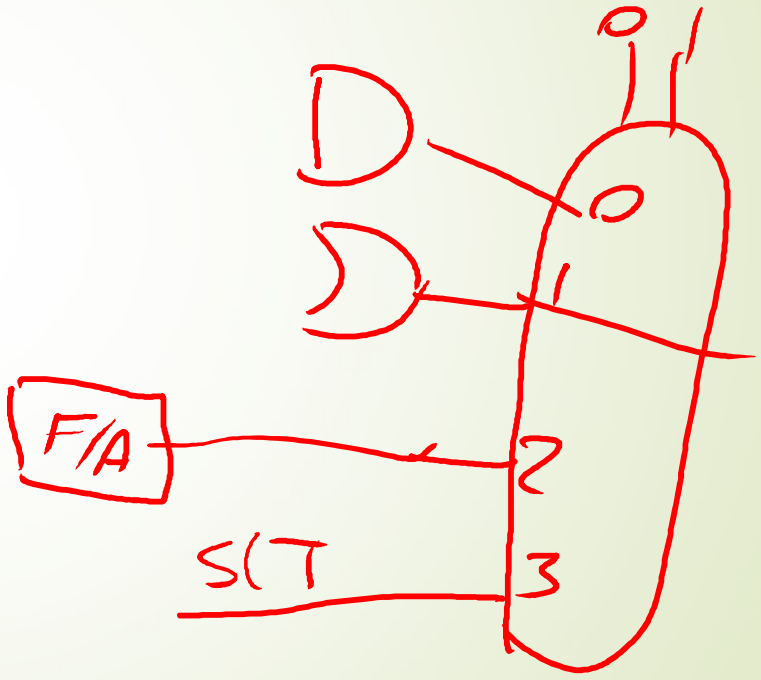
Instruction[5:0] (the rightmost bits) → Function field

1) If the instruction is OR, then the ALU control will (after examining the ALUOp and funct bits) output _____.

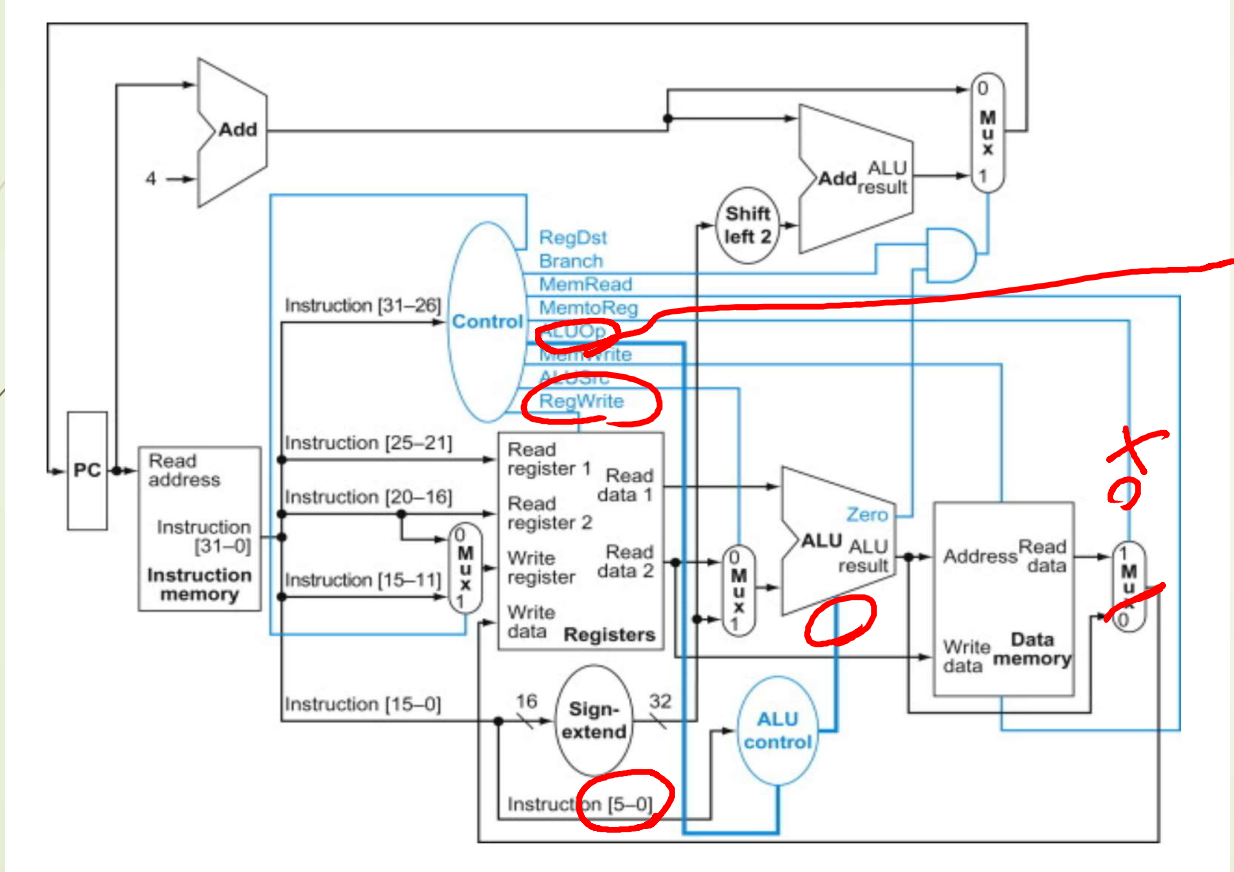
10

0000

0001 ← ALU designed



Consider the datapath and control unit below,



lw $sw 00
Beq 01
R 10

1) The control unit sends _____ bits to the ALU control.
0
1
2

1) The control unit enables a write to the register file using the _____ signal.
RegDst
MemWrite
RegWrite

1) When MemToReg is 0, the data appearing at the register file's data input comes from the _____.
ALU's output
data memory's output
register file's output

1) The ALU's top input always comes from the Read data 1 output of the register file. The ALU's bottom input can come from two possible places: The Read data 2 output of the register file, or the instruction's lower 16 bits, sign extended to 32 bits. Which control unit output select among those two places?
ALUOp
ALUSrc
Zero

13) The control unit's Branch output will be 1 for a branch equal instruction. However, the branch's target address is only loaded into the PC if the ALU's Zero output is _____. Otherwise, PC is loaded with PC + 4.
0
1

Consider the figure below showing control unit outputs for four kinds of instructions, using four rows (Rows 1, 2, 3, and 4).

Instruction	RegDst	ALUSrc	Memto-Reg	Reg-Write	Mem-Read	Mem-Write	Branch	ALUOp1	ALUOp0
R-format	1	0	0	1	0	0	0	1	0
lw	0	1	1	1	1	0	0	0	0
sw	X	1	X	0	0	1	0	0	0
beq	X	0	X	0	0	0	1	0	1

1) In Row 1, RegWrite is 1, meaning the register is always written for an R-type instruction.

True

False

1) In Row 1, the last two bits, ALUOp, are 10, meaning the ALU will perform an add function.

True

False

look into function to determine the operation

1) MemWrite is 1 for Row 3 (SW), but is 0 for Row 2. The reason is because while a store word instruction writes to the data memory, a ____ instruction does not.

R-type

load word

1) In beq's Row 4, MemToReg is X because the value appearing at the register file's Write data input is irrelevant.

True

False

Consider the datapath in action for a load instruction. Indicate the values for the listed control signals.

1) RegDst
0
1

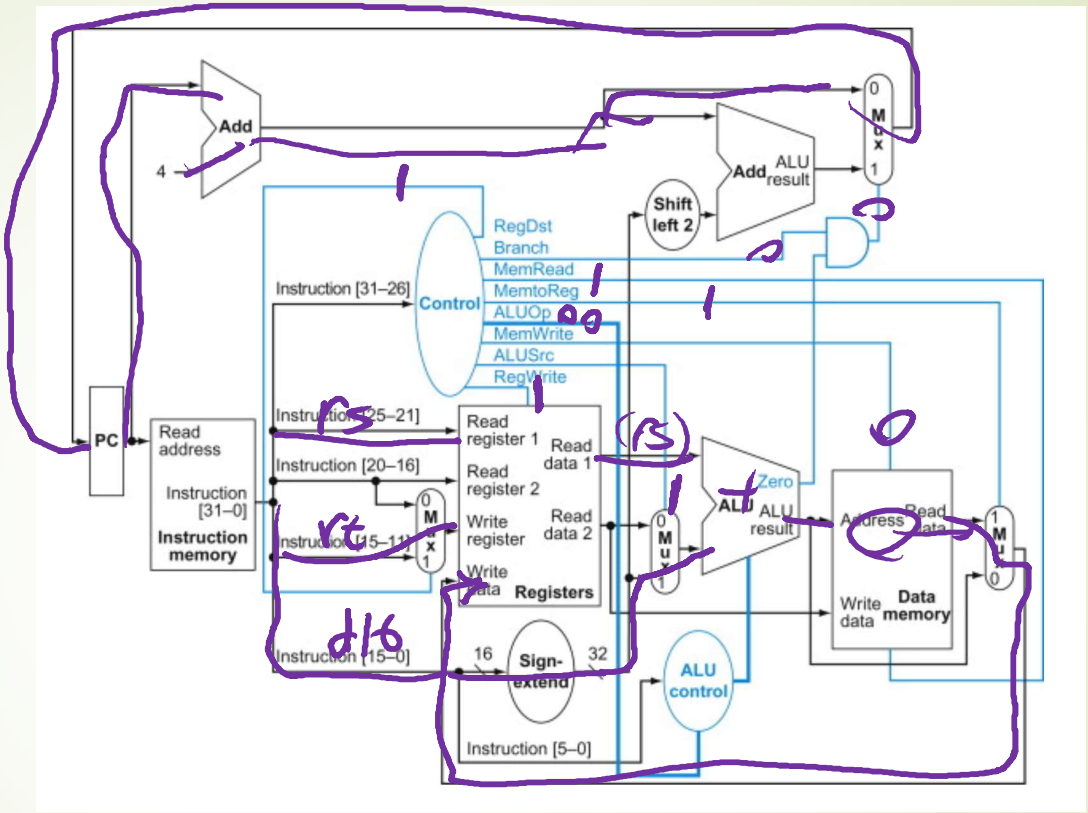
1) Branch
0
1

1) MemRead
0
1

1) MemToReg
0
1

1) ALUSrc
0
1

1) RegWrite
0
1

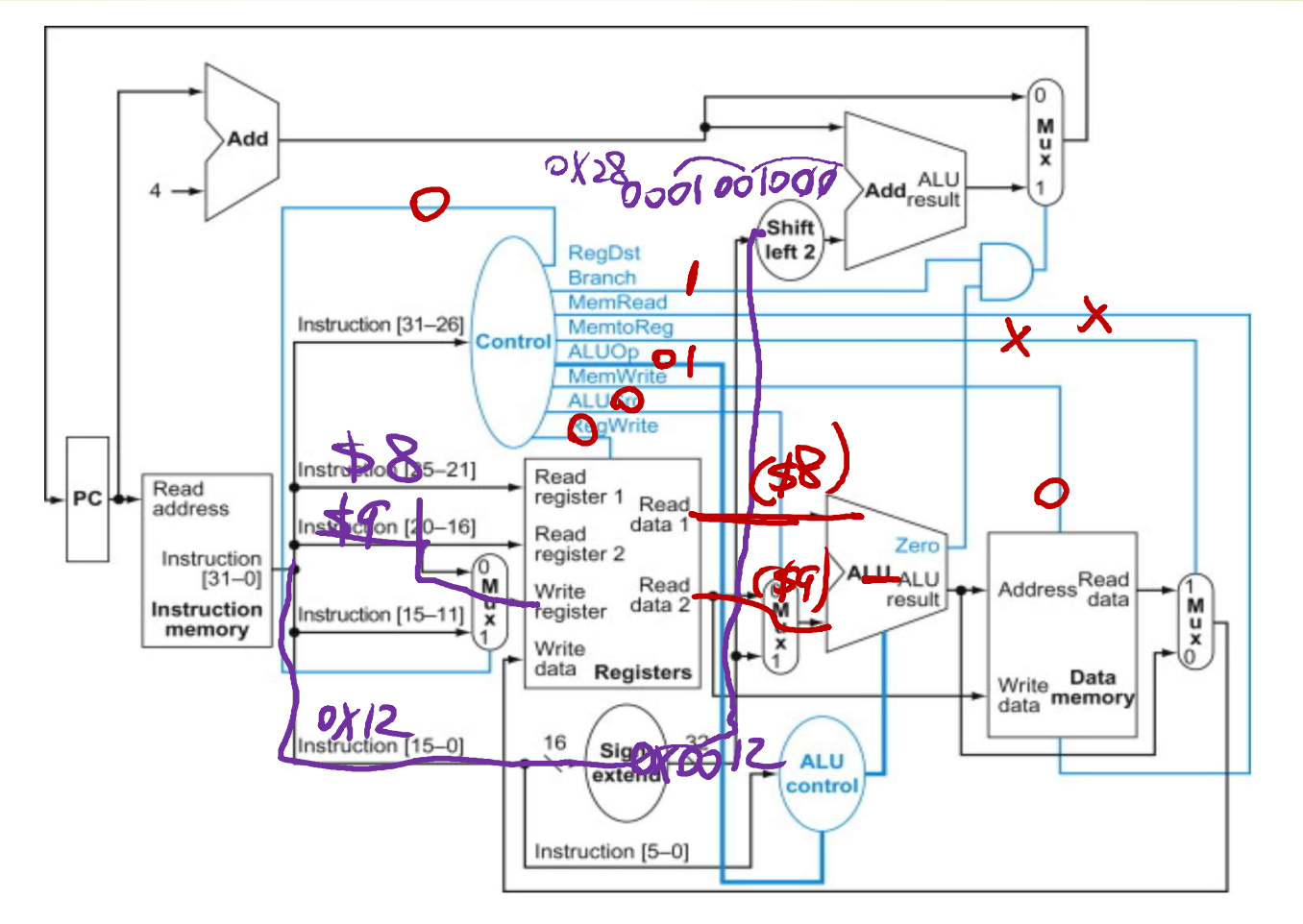


1) For a store word (SW) instruction, MemRead would be ____.
0
1

1) For a store word (SW) instruction, RegWrite would be ____.
0
1

1) Highlight the active paths and assign values to the control signals of the following for

a. beq $8, $9, 0x12



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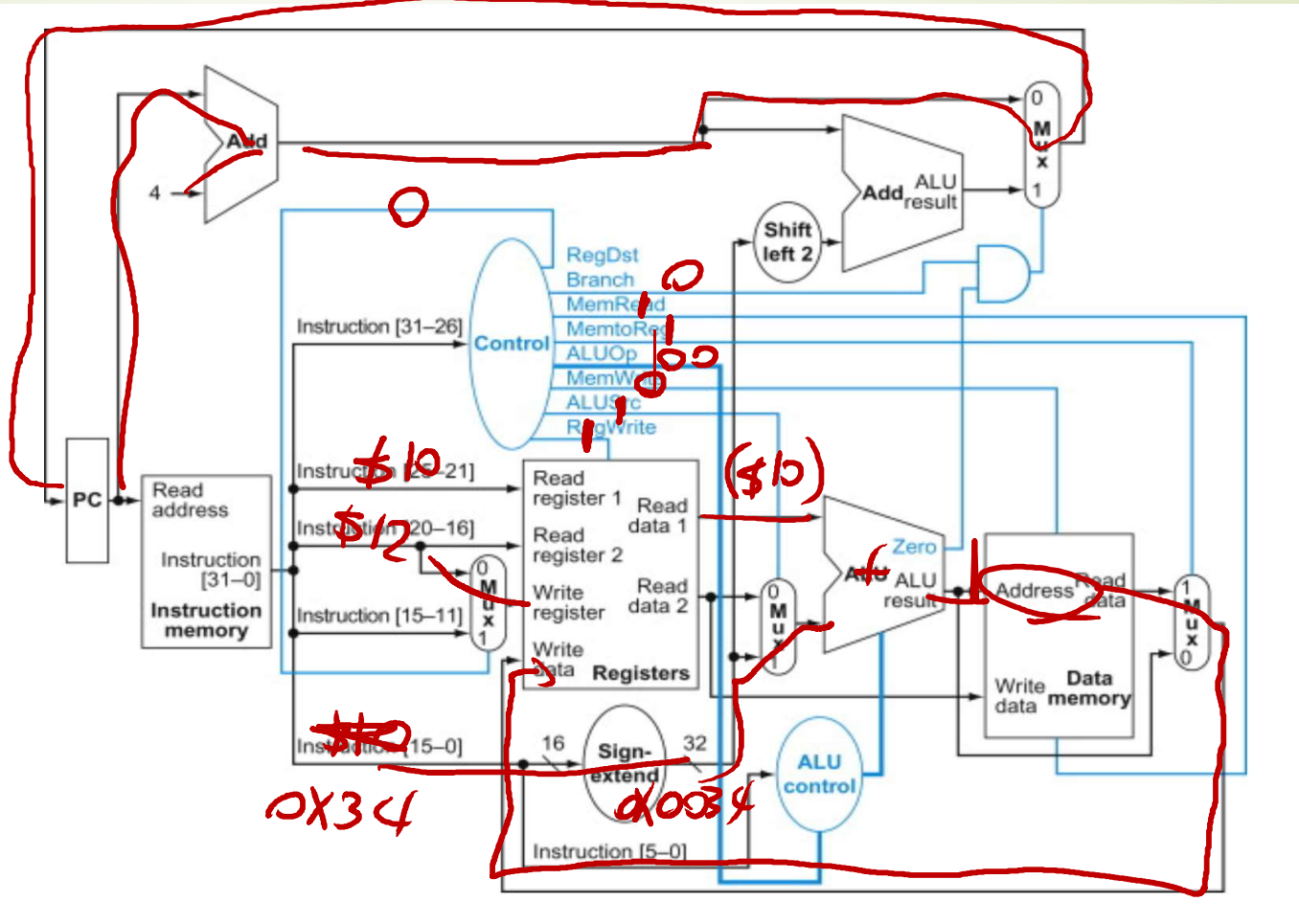
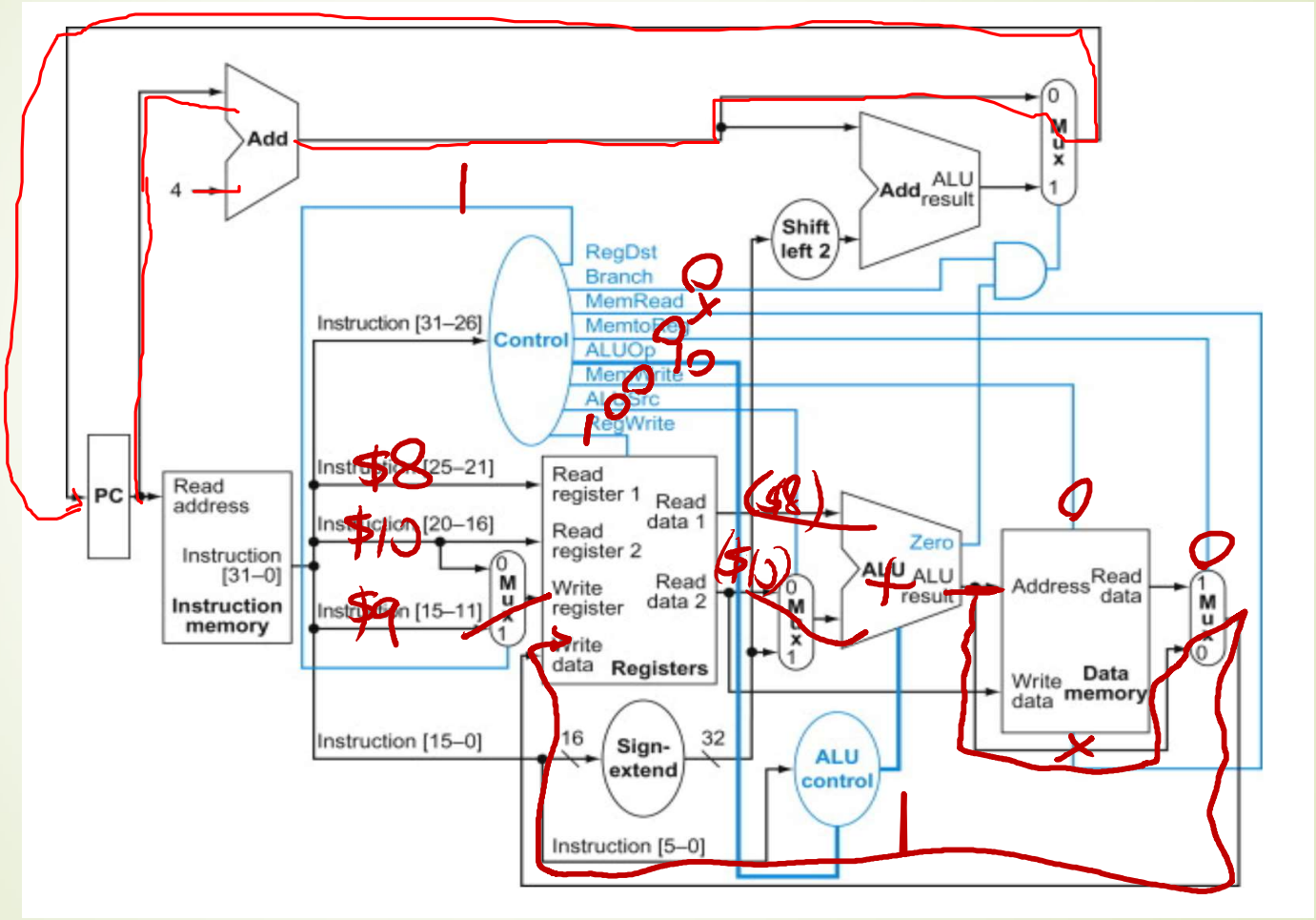
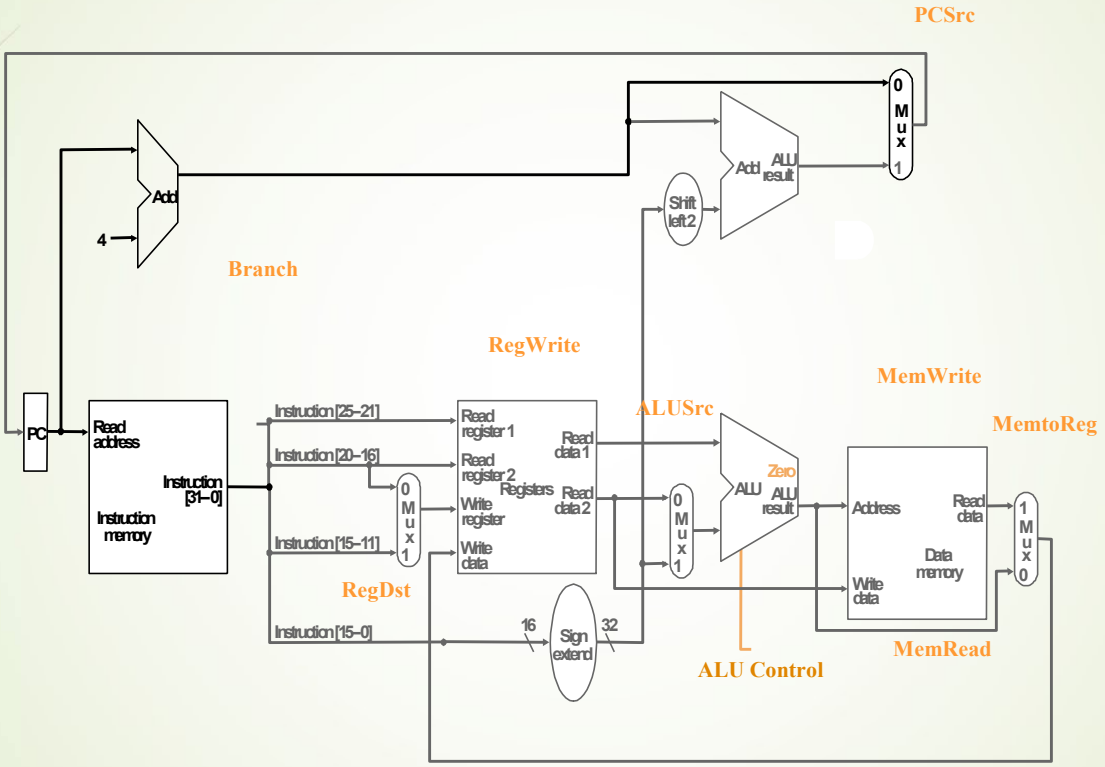


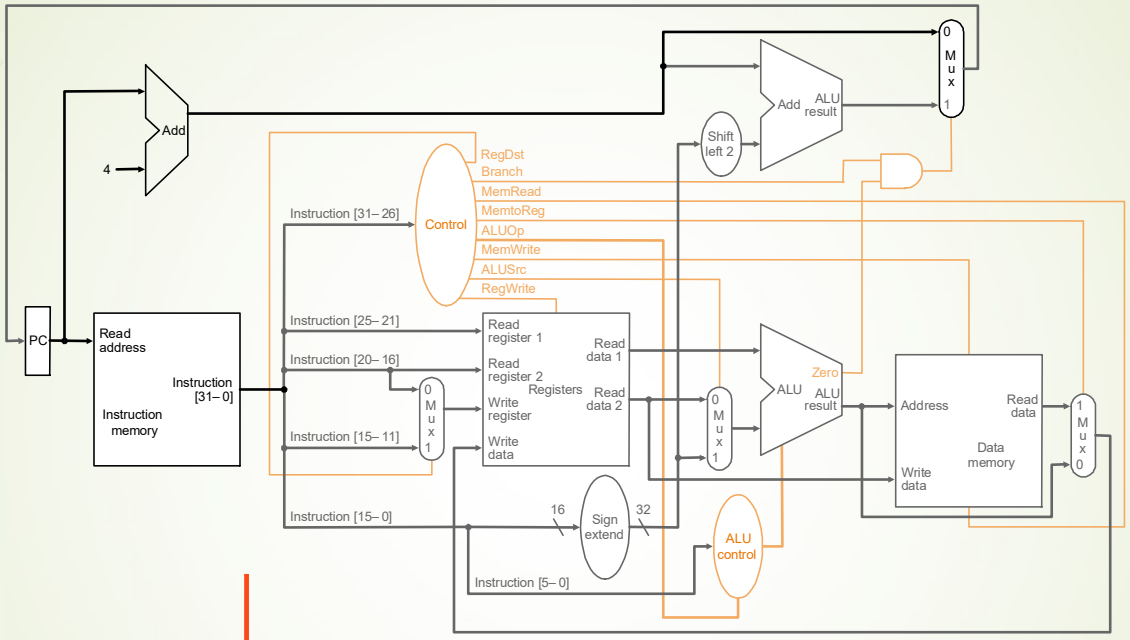
1) Highlight the active paths and assign values to the control signals of the following for

a. add $9, $8, $10




PCSrc
Add
4
Branch
0
M
u
x
1
Add
ALU result
Shift left 2
RegWrite
MemWrite
ALUSrc
MemtoReg
PC
Read address
Instruction [31–0]
Instruction memory
Instruction [25–21]
Instruction [20–16]
Instruction [15–11]
Instruction [15–0]
Read register 1
Read register 2
Registers
Write register
Write data
Read data 1
Read data 2
RegDst
16
Sign extend
32
ALU
Zero
ALU result
ALU Control
Address
Read data
Data memory
Write data
MemRead
1
M
u
x
0

Control



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R-format	00 0000	1	0	0	1	0	0	0	1	0
lw	10 0011	0	1	1	1	1	0	0	0	0
sw	10 1011	X	1	X	0	0	1	0	0	0
beq	00 0100	X	0	X	0	0	0	1	0	1

Single Cycle Control

- Simple combinational logic